IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra		
Assignee:	Lumileds Lighting U.S. LLC		
Title:	Forming Low Resistivity P-Type Gallium Nitride		
Serial No.:	09/846,980	Filing Date:	April 30, 2001
Examiner:	Matthew J. Song	Group Art Unit:	1765
Docket No.:	M-9635 US		

San Jose, California
April 6, 2004

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Commissioner for Patents
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Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 CFR § 1.191

Dear Sir:

Applicants submit this Appeal Brief pursuant to the Notice of Appeal filed in this case on December 8, 2003. The Commissioner is hereby authorized to deduct from Deposit Account No. 502226 the amount $330.00 specified in 37 CFR 1.17(c) for this Appeal Brief. Applicants respectfully petition for a 2-months extension of time, such extension allowing the undersigned until April 8, 204 to file the Appeal Brief. The Commissioner is hereby authorized to deduct the amount of $420.00 from Deposit Account No. 502226 for the extension of time. The Commissioner is also authorized to deduct any other amounts required for this appeal brief and to credit any amounts overpaid to Deposit Account No. 502226. This paper is submitted in triplicate.

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I. REAL PARTY IN INTEREST

The real partying interest is the assignee, Lumileds Lighting U.S. LLC, as named in the caption above.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 and 3-60 are pending in the present application, all of which stand rejected. Claim 2 is canceled. Claims 1 and 3-60 are hereby appealed.

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V. SUMMARY OF THE INVENTION

One important class of light emitting diodes is based upon compounds of group III atoms (particularly In, Ga, Al) with nitrogen N, typically abbreviated as "III-nitride." Such devices often include an active layer disposed between at least one n-type layer and at least one p-type layer. When the device is forward biased, the recombination of holes and electrons in the active layer results in emission of light of a wavelength determined by the structure and composition of the active layer. (Specification, page 1, lines 13-15, page 1, line 27 to page 2, line 8)

Although forming low resistivity n-type III-nitride materials is relatively easy, forming p-type III-nitride materials with low resistivity has proven difficult. In a typical process for forming the various III-nitride epitaxial layers, NH_3 (ammonia) gas is introduced into a chamber during a metalorganic chemical vapor deposition (MOCVD) process to contribute

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the N component, while other gases are introduced to contribute the Group III components and the p-type dopant, typically magnesium (Mg). During growth of the Mg-doped III-nitride material, some of the hydrogen atoms from the reaction gases are incorporated in the epitaxial layers and form a complex with the Mg dopants. This passivates the Mg acceptors, effectively neutralizing the effect of the Mg dopants as acceptors. (Specification, page 2, lines 18-27)

One aspect of the invention provides a method of manufacturing a p-type III-V nitride compound semiconductor. (Claim 1, Fig. 3, Specification page 5, line 21 to page 8, line 25) The method comprises: growing (30) in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into the layer to form an acceptor-doped layer, the chamber containing a gas providing hydrogen that passivates at least some of the acceptor impurities; cooling (36) the acceptor-doped layer to a second temperature lower than the first temperature; preventing additional hydrogen from diffusing into the acceptor-doped layer substantially during cooling; causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer thereby increasing the hole density and lowering the resistivity of the p-type layer.

Another aspect of the invention provides a method of manufacturing a p-type III-V nitride compound semiconductor. (Claim 1, Fig. 3, Specification page 5, line 21 to page 8, line 25) The method comprises: growing (30) in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into the layer to form an acceptor-doped layer, the chamber containing a gas providing hydrogen that passivates at least some of the acceptor impurities; cooling (36) the acceptor-doped layer to a

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second temperature significantly lower than the first temperature, thereby causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer, thereby increasing said hole density and lowering the resistivity of said p-type layer.

VI. ISSUES

Whether claims 1 and 3-60 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Bour et al., U.S. Patent No. 5,926,726 in view of Koike et al., U.S. Patent No. 5,811,319 and Furukawa et al., U.S. Patent 6,017,807.

VII. GROUPING OF THE CLAIMS

Claims 1 and 3-60 stand or fall together.

VIII. ARGUMENTS

Claims 1, 3-5, 12-35 and 42-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bour et al., U.S. Patent No. 5,926,726 (hereinafter "Bour") in view of Koike et al., U.S. Patent No. 5,811,319 (hereinafter "Koike") and Furukawa et al., U.S. Patent 6,017,807 (hereinafter "Furukawa"). The Examiner uses Bour as a base reference, cites Koike as teaching a particular hole concentration, and cites Furukawa as teaching a thermal anneal.

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Claims 1 and 31 recite "growing in a chamber a III-V nitride compound semiconductor layer at a first temperature . . . cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process . . . and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C." Emphasis added.

In the office action mailed August 6, 2003 and the office action mailed February 24, 2003, the Examiner describes a Bour/Furukawa combination as follows. Furukawa is cited as teaching a thermal anneal to activate the p-type impurities in the device:

> Bour et al also does not teach heating said p-type layer to a third temperature greater than the second temperature and less than 625°C.
> In a method of forming a P-type GaN compound, note entire reference, Furukawa et al teaches after a p-type gallium nitride compound semiconductor layers formed by chemical vapor deposition, the p-type gallium nitride layers are thermally annealed at more than 400°C and the p-type impurity can be more effectively activated so that p-type gallium nitride compound semiconductor layers which have fewer crystal defects and lower resistivity can be formed (abstract, col 4, ln 5-67 and col 6, ln 35-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bour et al with Furukawa et al annealing at a temperature greater than 400°C to form a semiconductor layer which has fewer defects and lower resistivity.

In response, in the office action response mailed May 22, 2003, Applicants argued that Bour teaches away from combination with Furukawa, because Bour's method is specifically designed to avoid the use of a post-cool-down anneal as described in Furukawa:

> It would not have been obvious to modify Bour's process to add an anneal after cool-down is complete, as taught by Furukawa, because Bour specifically teaches that it is undesirable to complete cool-down prior to performing an anneal. See, for example, column 3, lines 46-50 of Bour which list problems associated with such a post-cool-down anneal including high processing costs, and potential contamination from exposure to the atmosphere accompanying ex-situ processing. Even if the post-cool-down anneal is performed in situ, a person of skill in the art would still expect to encounter high processing times and costs and potential contamination, and would therefore not be motivated to modify Bour's process.
>
> MPEP section 2141 teaches "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: . . . The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination." Bour's entire teaching is devoted to providing a process that avoids the use of a post-cool-down anneal, and thus cannot possibly suggest the desirability of combining Bour with a reference that uses a post-cool-down anneal. Since Bour specifically teaches away from providing a post-cool-down anneal, Bour cannot be combined with any reference that teaches such an anneal, including Furukawa. (Emphasis in original)

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In response, the Examiner states that though Bour teaches a process that does not require a post growth anneal, a post growth anneal would be expected to increase activation yield of a p-type layer, and thus would be a favorable addition to Bour's process:

> Applicant's argument that it would not have been obvious to combine Furukawa with Bour has been noted but is not found persuasive. Applicant alleges Bour specifically teaches that it is undesirable to complete cool-down prior to performing an anneal because of high processing times and costs, therefore Bour cannot be combined with Furukawa, which teaches a post cool down anneal. Bour does teach a process that does not require a post growth acceptor activation process, note column 9, lines 1-3, as suggest by applicant, which would reduce processing costs. Bour also recognizes post growth anneals after reactor cool down are common procedure, note column 2, lines 60-65. Furukawa teaches the activation yield of a p-type impurity can be improved by a simple process by annealing at more than 400°C in an inert atmosphere, note column 2, line 60 to column 3, line 10. Bour teaches a process without a post growth anneal to reduce cost and Furukawa teaches a post growth anneal to improve the activation yield of a p-type impurity. Although, the processing cost would increase because of a post growth anneal; a person of ordinary skill in that art at the time of the invention would be motivated to perform a post growth anneal to improve the activation yield. Economics are a concern in all processes; however obtaining a superior product (increased activation yield) is a valid motivation for increasing processing costs.

The Examiner's position that the language in Bour teaching away from combination with Furukawa can be "overcome" ignores the plan language of MPEP section 2145 X D 2, which states that "references cannot be combined where reference teaches away from their combination." See also, for example, Tec Air, Inc. v. Denso Mfg. Michigan Inc., 192 F.3d 1353, 1359, which states "[t]here is no suggestion to combine, however, if a reference teaches away from its combination with another source." The above-quoted MPEP section and case law clearly state that a combination of references cannot be made where one of the references teaches away from combination with the other. Thus, since Applicant has cited language in Bour that clearly teaches away from combination with Furukawa, Bour cannot properly be combined with Furukawa.

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Claims 6-11, 13, 36-39, 41, 43, and 50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bour, Koike, and Furukawa, in view of various other references. Each of

the other references is directed to a limitation present in the dependent claims, and as such these references add nothing to the deficiencies of Bour and Furukawa, argued above.

IX. CONCLUSION

For the above reasons, Applicants respectfully submit that the rejection of pending claims 1 and 3-60 is unfounded. Accordingly, Applicants request that the rejection be reversed.

Certification of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

R Leiterman 4/6/04
Signature Date

Respectfully submitted,

R Leiterman

Rachel V. Leiterman
Attorney for Applicants
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APPENDIX

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially during the cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

3. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

4. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a

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p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than

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$5x10^{18}cm^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.

19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

31. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

32. The method of Claim 31 further comprising substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

33. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

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34. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

35. The method of Claim 31 further comprising treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

36. The method of Claim 35 wherein said treating said surface comprises chemically etching said surface.

37. The method of Claim 35 wherein said treating said surface comprises plasma etching said surface.

38. The method of Claim 35 wherein said treating said surface comprises plasma cleaning said surface.

39. The method of Claim 35 wherein said treating said surface comprises chemically cleaning said surface.

40. The method of Claim 39 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

41. The method of Claim 35 wherein said treating said surface comprises ultrasonically cleaning said surface.

42. The method of Claim 35 wherein said treating said surface comprises irradiating said surface with an electron-beam.

43. The method of Claim 35 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

44. The method of Claim 31 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

45. The method of Claim 31 wherein, after said cool-down process, said hole

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density is greater than $3x10^{16}cm^{-3}$.

46. The method of Claim 31 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

47. The method of Claim 31 wherein said annealing is carried out at a temperature in the range of 100-625°C.

48. The method of Claim 31 wherein said annealing is carried out at a temperature below 400°C.

49. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

50. The method of Claim 31 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

51. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

52. The method of Claim 51 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

53. The method of Claim 31 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

54. The method of Claim 31 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

55. The method of Claim 31 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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To:	**U.S. Patent and Trademark Office**	**Phone:**	**703-306-5665**
	Mail Stop AF **Commissioner for Patents** **P. O. Box 1450** **Alexandria, VA 22313-1450**		
From:	**Rachel V. Leiterman**		
Serial No.:	**09/846,980**		
Docket:	**M-9635 US** **(LUM- M-9635 US)**		
Re:	**Appeal Brief**		
Pages:	**45 (including cover sheet)**		

Message:

Re: Applicant(s): Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra
Assignee: Lumileds Lighting U.S., LLC
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Transmitted herewith are the following documents in the above-identified application:

(1) Transmittal Letter (1 page in duplicate);
(2) Appeal Brief (14 pages in triplicate).

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the N component, while other gases are introduced to contribute the Group III components and the p-type dopant, typically magnesium (Mg). During growth of the Mg-doped III-nitride material, some of the hydrogen atoms from the reaction gases are incorporated in the epitaxial layers and form a complex with the Mg dopants. This passivates the Mg acceptors, effectively neutralizing the effect of the Mg dopants as acceptors. (Specification, page 2, lines 18-27)

One aspect of the invention provides a method of manufacturing a p-type III-V nitride compound semiconductor. (Claim 1, Fig. 3, Specification page 5, line 21 to page 8, line 25) The method comprises: growing (30) in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into the layer to form an acceptor-doped layer, the chamber containing a gas providing hydrogen that passivates at least some of the acceptor impurities; cooling (36) the acceptor-doped layer to a second temperature lower than the first temperature; preventing additional hydrogen from diffusing into the acceptor-doped layer substantially during cooling; causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer thereby increasing the hole density and lowering the resistivity of the p-type layer.

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second temperature significantly lower than the first temperature, thereby causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer, thereby increasing said hole density and lowering the resistivity of said p-type layer.

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Claims 1 and 31 recite "growing in a chamber a III-V nitride compound semiconductor layer at a first temperature . . . cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process . . . and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C." Emphasis added.

In the office action mailed August 6, 2003 and the office action mailed February 24, 2003, the Examiner describes a Bour/Furukawa combination as follows. Furukawa is cited as teaching a thermal anneal to activate the p-type impurities in the device:

> Bour et al also does not teach heating said p-type layer to a third temperature greater than the second temperature and less than 625°C.
> In a method of forming a P-type GaN compound, note entire reference, Furukawa et al teaches after a p-type gallium nitride compound semiconductor layers formed by chemical vapor deposition, the p-type gallium nitride layers are thermally annealed at more than 400°C and the p-type impurity can be more effectively activated so that p-type gallium nitride compound semiconductor layers which have fewer crystal defects and lower resistivity can be formed (abstract, col 4, ln 5-67 and col 6, ln 35-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bour et al with Furukawa et al annealing at a temperature greater than 400°C to form a semiconductor layer which has fewer defects and lower resistivity.

In response, in the office action response mailed May 22, 2003, Applicants argued that Bour teaches away from combination with Furukawa, because Bour's method is specifically designed to avoid the use of a post-cool-down anneal as described in Furukawa:

> It would not have been obvious to modify Bour's process to add an anneal after cool-down is complete, as taught by Furukawa, because Bour specifically teaches that it is undesirable to complete cool-down prior to performing an anneal. See, for example, column 3, lines 46-50 of Bour which list problems associated with such a post-cool-down anneal including high processing costs, and potential contamination from exposure to the atmosphere accompanying ex-situ processing. Even if the post-cool-down anneal is performed in situ, a person of skill in the art would still expect to encounter high processing times and costs and potential contamination, and would therefore not be motivated to modify Bour's process.
>
> MPEP section 2141 teaches "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: . . . The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination." Bour's entire teaching is devoted to providing a process that avoids the use of a post-cool-down anneal, and thus cannot possibly suggest the desirability of combining Bour with a reference that uses a post-cool-down anneal. Since Bour specifically teaches away from providing a post-cool-down anneal, Bour cannot be combined with any reference that teaches such an anneal, including Furukawa. (Emphasis in original)

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In response, the Examiner states that though Bour teaches a process that does not require a post growth anneal, a post growth anneal would be expected to increase activation yield of a p-type layer, and thus would be a favorable addition to Bour's process:

> Applicant's argument that it would not have been obvious to combine Furukawa with Bour has been noted but is not found persuasive. Applicant alleges Bour specifically teaches that it is undesirable to complete cool-down prior to performing an anneal because of high processing times and costs, therefore Bour cannot be combined with Furukawa, which teaches a post cool down anneal. Bour does teach a process that does not require a post growth acceptor activation process, note column 9, lines 1-3, as suggest by applicant, which would reduce processing costs. Bour also recognizes post growth anneals after reactor cool down are common procedure, note column 2, lines 60-65. Furukawa teaches the activation yield of a p-type impurity can be improved by a simple process by annealing at more than 400°C in an inert atmosphere, note column 2, line 60 to column 3, line 10. Bour teaches a process without a post growth anneal to reduce cost and Furukawa teaches a post growth anneal to improve the activation yield of a p-type impurity. Although, the processing cost would increase because of a post growth anneal; a person of ordinary skill in that art at the time of the invention would be motivated to perform a post growth anneal to improve the activation yield. Economics are a concern in all processes; however obtaining a superior product (increased activation yield) is a valid motivation for increasing processing costs.

The Examiner's position that the language in Bour teaching away from combination with Furukawa can be "overcome" ignores the plan language of MPEP section 2145 X D 2, which states that "references cannot be combined where reference teaches away from their combination." See also, for example, Tec Air, Inc. v. Denso Mfg. Michigan Inc., 192 F.3d 1353, 1359, which states "[t]here is no suggestion to combine, however, if a reference teaches away from its combination with another source." The above-quoted MPEP section and case law clearly state that a combination of references cannot be made where one of the references teaches away from combination with the other. Thus, since Applicant has cited language in Bour that clearly teaches away from combination with Furukawa, Bour cannot properly be combined with Furukawa.

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Claims 6-11, 13, 36-39, 41, 43, and 50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bour, Koike, and Furukawa, in view of various other references. Each of

the other references is directed to a limitation present in the dependent claims, and as such these references add nothing to the deficiencies of Bour and Furukawa, argued above.

IX. CONCLUSION

For the above reasons, Applicants respectfully submit that the rejection of pending claims 1 and 3-60 is unfounded. Accordingly, Applicants request that the rejection be reversed.

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R Leiterman 4/6/04

Signature Date

Respectfully submitted,

R Leiterman

Rachel V. Leiterman
Attorney for Applicants
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APPENDIX

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially during the cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

3. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

4. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a

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p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

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16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than

$5x10^{18}cm^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.

19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

31. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

32. The method of Claim 31 further comprising substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

33. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

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34. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

35. The method of Claim 31 further comprising treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

36. The method of Claim 35 wherein said treating said surface comprises chemically etching said surface.

37. The method of Claim 35 wherein said treating said surface comprises plasma etching said surface.

38. The method of Claim 35 wherein said treating said surface comprises plasma cleaning said surface.

39. The method of Claim 35 wherein said treating said surface comprises chemically cleaning said surface.

40. The method of Claim 39 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_40H.

41. The method of Claim 35 wherein said treating said surface comprises ultrasonically cleaning said surface.

42. The method of Claim 35 wherein said treating said surface comprises irradiating said surface with an electron-beam.

43. The method of Claim 35 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

44. The method of Claim 31 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

45. The method of Claim 31 wherein, after said cool-down process, said hole

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density is greater than $3x10^{16}cm^{-3}$.

46. The method of Claim 31 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

47. The method of Claim 31 wherein said annealing is carried out at a temperature in the range of 100-625°C.

48. The method of Claim 31 wherein said annealing is carried out at a temperature below 400°C.

49. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

50. The method of Claim 31 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

51. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

52. The method of Claim 51 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

53. The method of Claim 31 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

54. The method of Claim 31 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

55. The method of Claim 31 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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56. The method of Claim 31 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

57. The method of Claim 31 wherein said acceptor impurities comprise magnesium.

58. The method of Claim 31 wherein said annealing is carried out in a gas environment containing N_2.

59. The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

60. The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra		
Assignee:	Lumileds Lighting U.S. LLC		
Title:	Forming Low Resistivity P-Type Gallium Nitride		
Serial No.:	09/846,980	Filing Date:	April 30, 2001
Examiner:	Matthew J. Song	Group Art Unit:	1765
Docket No.:	M-9635 US		

San Jose, California
April 6, 2004

Mail Stop AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 CFR § 1.191

Dear Sir:

Applicants submit this Appeal Brief pursuant to the Notice of Appeal filed in this case on December 8, 2003. The Commissioner is hereby authorized to deduct from Deposit Account No. 502226 the amount $330.00 specified in 37 CFR 1.17(c) for this Appeal Brief. Applicants respectfully petition for a 2-months extension of time, such extension allowing the undersigned until April 8, 204 to file the Appeal Brief. The Commissioner is hereby authorized to deduct the amount of $420.00 from Deposit Account No. 502226 for the extension of time. The Commissioner is also authorized to deduct any other amounts required for this appeal brief and to credit any amounts overpaid to Deposit Account No. 502226. This paper is submitted in triplicate.

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I. REAL PARTY IN INTEREST

The real partying interest is the assignee, Lumileds Lighting U.S. LLC, as named in the caption above.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 and 3-60 are pending in the present application, all of which stand rejected. Claim 2 is canceled. Claims 1 and 3-60 are hereby appealed.

IV. STATUS OF AMENDMENTS

On October 3, 2003, Appellant submitted a Request for Reconsideration. No claims were amended in that request. The Examiner issued an Advisory Action on October 20, 2003.

V. SUMMARY OF THE INVENTION

One important class of light emitting diodes is based upon compounds of group III atoms (particularly In, Ga, Al) with nitrogen N, typically abbreviated as "III-nitride." Such devices often include an active layer disposed between at least one n-type layer and at least one p-type layer. When the device is forward biased, the recombination of holes and electrons in the active layer results in emission of light of a wavelength determined by the structure and composition of the active layer. (Specification, page 1, lines 13-15, page 1, line 27 to page 2, line 8)

Although forming low resistivity n-type III-nitride materials is relatively easy, forming p-type III-nitride materials with low resistivity has proven difficult. In a typical process for forming the various III-nitride epitaxial layers, NH_3 (ammonia) gas is introduced into a chamber during a metalorganic chemical vapor deposition (MOCVD) process to contribute

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the N component, while other gases are introduced to contribute the Group III components and the p-type dopant, typically magnesium (Mg). During growth of the Mg-doped III-nitride material, some of the hydrogen atoms from the reaction gases are incorporated in the epitaxial layers and form a complex with the Mg dopants. This passivates the Mg acceptors, effectively neutralizing the effect of the Mg dopants as acceptors. (Specification, page 2, lines 18-27)

One aspect of the invention provides a method of manufacturing a p-type III-V nitride compound semiconductor. (Claim 1, Fig. 3, Specification page 5, line 21 to page 8, line 25) The method comprises: growing (30) in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into the layer to form an acceptor-doped layer, the chamber containing a gas providing hydrogen that passivates at least some of the acceptor impurities; cooling (36) the acceptor-doped layer to a second temperature lower than the first temperature; preventing additional hydrogen from diffusing into the acceptor-doped layer substantially during cooling; causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer thereby increasing the hole density and lowering the resistivity of the p-type layer.

Another aspect of the invention provides a method of manufacturing a p-type III-V nitride compound semiconductor. (Claim 1, Fig. 3, Specification page 5, line 21 to page 8, line 25) The method comprises: growing (30) in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into the layer to form an acceptor-doped layer, the chamber containing a gas providing hydrogen that passivates at least some of the acceptor impurities; cooling (36) the acceptor-doped layer to a

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second temperature significantly lower than the first temperature, thereby causing the acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after cooling; and after cooling, heating (38) the p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from the p-type layer, thereby increasing said hole density and lowering the resistivity of said p-type layer.

VI. ISSUES

Whether claims 1 and 3-60 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Bour et al., U.S. Patent No. 5,926,726 in view of Koike et al., U.S. Patent No. 5,811,319 and Furukawa et al., U.S. Patent 6,017,807.

VII. GROUPING OF THE CLAIMS

Claims 1 and 3-60 stand or fall together.

VIII. ARGUMENTS

Claims 1, 3-5, 12-35 and 42-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bour et al., U.S. Patent No. 5,926,726 (hereinafter "Bour") in view of Koike et al., U.S. Patent No. 5,811,319 (hereinafter "Koike") and Furukawa et al., U.S. Patent 6,017,807 (hereinafter "Furukawa"). The Examiner uses Bour as a base reference, cites Koike as teaching a particular hole concentration, and cites Furukawa as teaching a thermal anneal.

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R Leiterman 4/6/04
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Respectfully submitted,

R Leiterman

Rachel V. Leiterman
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APPENDIX

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

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cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially during the cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

3. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

4. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a

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p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

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16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than

$5x10^{18}cm^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.

19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

31. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

32. The method of Claim 31 further comprising substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

33. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

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34. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

35. The method of Claim 31 further comprising treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

36. The method of Claim 35 wherein said treating said surface comprises chemically etching said surface.

37. The method of Claim 35 wherein said treating said surface comprises plasma etching said surface.

38. The method of Claim 35 wherein said treating said surface comprises plasma cleaning said surface.

39. The method of Claim 35 wherein said treating said surface comprises chemically cleaning said surface.

40. The method of Claim 39 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

41. The method of Claim 35 wherein said treating said surface comprises ultrasonically cleaning said surface.

42. The method of Claim 35 wherein said treating said surface comprises irradiating said surface with an electron-beam.

43. The method of Claim 35 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

44. The method of Claim 31 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

45. The method of Claim 31 wherein, after said cool-down process, said hole

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density is greater than $3x10^{16}cm^{-3}$.

46. The method of Claim 31 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

47. The method of Claim 31 wherein said annealing is carried out at a temperature in the range of 100-625°C.

48. The method of Claim 31 wherein said annealing is carried out at a temperature below 400°C.

49. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

50. The method of Claim 31 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

51. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

52. The method of Claim 51 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

53. The method of Claim 31 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

54. The method of Claim 31 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

55. The method of Claim 31 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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56. The method of Claim 31 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

57. The method of Claim 31 wherein said acceptor impurities comprise magnesium.

58. The method of Claim 31 wherein said annealing is carried out in a gas environment containing N_2.

59. The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

60. The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

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